HP 13255

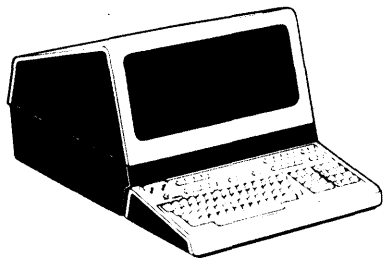
SYNCHRONOUS MULTIPOINT INTERFACE MODULE

Manual Part No. 13255-91107

PRINTED

AUG-01-76

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The Synchronous Multipoint Interface Module performs data serialization and control for EIA RS232C compatible interfacing. Circuitry is provided allowing data, clock, and control to be buffered and sent to additional 264XX terminals with the Syncnronous Multipoint Interface PCA in a daisy-chain line sharing configuration (for polled multipoint operation). Parts lists for the cables and Self Test Connector Assembly (5061-2403, 5061-2409, 02640-60132, 02640-60133, 02640-60134, 02640-60140, and 02645-60004) are covered in module section 13255-91106. Parts lists for the Data Comm Self Test Hood (02640-60002) and US Modem Cable Assembly (02640-60131) are covered in module section 13255-91086.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Synchronous Multipoint Interface Module is contained in tables 1.0 through 6.8.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
5061-2403	Modem Bypass Cable Ass'y	N/A	N/A
5061-2409	European Modem Cable Ass'y	N/A	N/A
02640-60107	Synchronous Multipoint Interface PCA	12.9 x 4.0 x 0.6	0.50
02640-60131	US Modem Cable Assembly	N/A	N/A
02640-60132	Modem Multipoint Cable Ass'y	N/A	N/A
02640-60133	Multipoint Cable Ass'y	N/A	N/A
02640-60134	Multipoint Extension Cable Assembly	N/A	N/A
02640-60140	Power Down Protect PCA	N/A	N/A
02645-60002	Data Comm Self Test Hood	N/A	N/A
02645-60004	Self Test Connector Ass'y	N/A	N/A

Number of Backplane Slots Required: 1

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

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02640-60132	Modem Multipoint Cable Ass'y	N/A	N/A
02640-60133	Multipoint Cable Ass'y	N/A	N/A
02640-60134	Multipoint Extension Cable Assembly	N/A	N/A
02640-60140	Power Down Protect PCA	N/A	N/A
02645-60002	Data Comm Self Test Hood	N/A	N/A
02645-60004	Self Test Connector Ass'y	N/A	N/A

Number of Backplane Slots Required: 1

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 1.998 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	+42 Volt Supply
@ 400 mA	@ 200 mA	@ 50 mA (An additional 200 mA required for 02640-60140 cable)	@ mA NOT APPLICABLE
115 volts ac @ A NOT APPLICABLE		220 volts ac @ A NOT APPLICABLE	
Clock Frequency: 4.915 MHz			

Table 4.0 Switch Definitions

PCA Designation	Function	
	Open	Closed
J17-J10 J07-J00 (Software Configuration)	Jnn Bit = 1	Jnn Bit = 0
-12	Disconnects -12V from P2, Pin N	Connect -12V to P2, Pin N
A4 A9 A10 A11	Address Bit is a "1" in the module address	Address Bit is a "0" in the module address
RCLK	Does not connect RCLK to DD P2, Pin 13	Connect RCLK to DD P2, Pin 13
2400,4800, 9600, 19K	If all are open no clock will be present on clock Pin DA (P2, Pin 5) and RCLK	Close only one. Selects Sync Clock Rate for RCLK and DA (P2, Pin S)

5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13		Not Used
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16		Not Used
-17		
-18		
-19		
-20		
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R		Not Used
-S	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		Not Used
-W		
-X		
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z	$\overline{\text{ATN}}$	Negative True, Data Comm Interrupt Request

5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	BAO	Data Out (output) - Active Driver
-2	CAO	Request to Send (output) - Active Driver
-3	BAI	Data Out (input) - Opto-Isolated Receiver
-4	CAI	Request to Send (input) - Opto-Isolated
-5	DBI	Transmit Clock (input) - Opto-Isolated
-6	DDO	Receive Clock (output) - Active Driver
-7	DBO	Transmit Clock (output) - Active Driver
-8	RET-D	Ground Return for BAI and CAI
-9	DDI	Receive Clock (input) - Opto-Isolated
-10	RET-I	Ground Return for BBI, CBI, DBI, DDI
-11	CBO	Clear to Send (output) - Active Driver
-12	DB	RS232C Transmit Clock (input)
-13	DD	RS232C Receive Clock (input)
-14	CE	RS232C Ring Indicator (input)
-15	BBO	Receive Data (output) - Active Driver

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P2, Pin A	AA	RS232C Frame Ground
-B	BA	RS232C Serial Data Out (output)
-C	BB	RS232C Serial Data In (input)
-D	CA	RS232C Request to Send (output)
-E	CB	RS232C Clear to Send (input)
-F	CC	RS232C Data Set Ready (input)
-H	AB	RS232C Signal Ground, Terminal Logic
-J	CF	RS232C Carrier Detect (input)
-K	BBI	Receive Data (input) - Opto-Isolated
-L	CBI	Clear to Send (input) - Opto-Isolated
-M	SCA	RS232C Secondary Request to Send (output)
-N	SCF	RS232C Secondary Cartridge Detect (input)
-P	CD	RS232C Data Terminal Ready (output)
-R	CH	RS232C Rate Select (output)
-S	DA	RS232C Transmit Clock (DTE output)

Table 6.0 Module Bus Pin Assignments

Function Performed: Output Sync Character for Transmit Fill Character and Receive Sync Character

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (A11 A10 A9 A4)
Switch Selectable
Data Comm = (1110)

Function Specifier: ADDR3 = 1
ADDR5 = 1
ADDR6 = 1

Data Bus Bit Interpretation:

B7
Output Sync Character Bit 7

B6
Output Sync Character Bit 6

B5
Output Sync Character Bit 5

B4
Output Sync Character Bit 4

B3
Output Sync Character Bit 3

B2
Output Sync Character Bit 2

B1
Output Sync Character Bit 1

B0
Output Sync Character Bit 0

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
A11	ADDR 11
A10	ADDR 10
A9	ADDR 9
X	ADDR 8
X	ADDR 7
1	ADDR 6
1	ADDR 5
A4	ADDR 4
1	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.1 Module Bus Pin Assignments

Function Performed: Output Data for Transmission	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11 A10 A9 A4)	X	ADDR 12
Switch Selectable	A11	ADDR 11
Data Comm = (1110)	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR3 = 0	X	ADDR 8
ADDR5 = 1	X	ADDR 7
ADDR6 = 1	1	ADDR 6
	1	ADDR 5
	A4	ADDR 4
Data Bus Bit Interpretation:	0	ADDR 3
	X	ADDR 2
B7	X	ADDR 1
Output Data Bit 7	X	ADDR 0
	B7	BUS 7
B6	B6	BUS 6
Output Data Bit 6	B5	BUS 5
	B4	BUS 4
B5	B3	BUS 3
Output Data Bit 5	B2	BUS 2
	B1	BUS 1
	B0	BUS 0
B4	1=Logical 1=Bus Low	
Output Data Bit 4	0=Logical 0=Bus High	
	X=Don't Care	
B3		
Output Data Bit 3		
B2		
Output Data Bit 2		
B1		
Output Data Bit 1		
B0		
Output Data Bit 0		

Table 6.2 Module Bus Pin Assignments

Function Performed: Output Control Byte 1 (Configuration Byte)

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (A11 A10 A9 A4)
Switch Selectable
Data Comm = (1110)

Function Specifier: ADDR5 = 1
ADDR6 = 0

Data Bus Bit Interpretation:

B6, B7 set number of data bits per character

	Data Bits 5	6	7	8
B7	0	0	1	1
B6	0	1	0	1

B5
0 = Enable Parity
1 = Inhibit Parity

B4
0 = Odd Parity
1 = Even Parity

B3 }
}
B2 }
} No Effect
B1 }
}
B0 }

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
A11	ADDR 11
A10	ADDR 10
A9	ADDR 9
X	ADDR 8
X	ADDR 7
0	ADDR 6
1	ADDR 5
A4	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.3 Module Bus Pin Assignments

Function Performed: Output Control byte 2 (Modem Control byte)	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11 A10 A9 A4)	X	ADDR 12
Data Comm = (1110)	A11	ADDR 11
	A10	ADDR 10
Function Specifier: ADDR5 = 0	A9	ADDR 9
ADDR6 = 1	X	ADDR 8
	X	ADDR 7
	1	ADDR 6
Data Bus Bit Interpretation:	0	ADDR 5
	A4	ADDR 4
B7	X	ADDR 3
0 = Enable Daisy-Chain CAI and CBO	X	ADDR 2
1 = Inhibit Daisy-Chain CAI and CBO	X	ADDR 1
	X	ADDR 0
B6	B7	BUS 7
Not Used	B6	BUS 6
	B5	BUS 5
B5	B4	BUS 4
Not Used	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
B4	B0	BUS 0
0 = Terminal Mode	1=Logical 1=Bus Low	
1 = Channel Monitor Mode	0=Logical 0=Bus High	
	X=Don't Care	
B3		
0 = CH On		
1 = CH Off		
B2		
0 = CD On		
1 = CD Off		
B1		
0 = SA On		
1 = SA Off		
B0		
0 = CA On		
1 = CA Off		

Table 6.4 Module Bus Pin Assignments

Function Performed: Output Control Bits	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11 A10 A9 A4)	X	ADDR 12
Switch Selectable	A11	ADDR 11
Data Comm = (1110)	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR5 = 0	X	ADDR 8
ADDR6 = 0	A7	ADDR 7
	0	ADDR 6
Only one bit in each of the pairs A0,A1 and A3,A7	0	ADDR 5
Can be set to "1" for a given output command	A4	ADDR 4
	A3	ADDR 3
	A2	ADDR 2
A0	A1	ADDR 1
0 = No Effect	A0	ADDR 0
1 = Reset Timer		
	B7	BUS 7
A1	B6	BUS 6
0 = No Effect	B5	BUS 5
1 = Set Timer	B4	BUS 4
	B3	BUS 3
A2	B2	BUS 2
0 = No Effect	B1	BUS 1
1 = USRT Receiver Reset (Sync Search and Clear Receiver Status)	B0	BUS 0
	1=Logical 1=Bus Low	
A3	0=Logical 0=Bus High	
0 = No Effect	X=Don't Care	
1 = Enable Transmission Complete Interrupt		
A7		
0 = No Effect		
1 = Enable Transmitter Ready Interrupt		
Data Bus Bit Interpretation: Not Applicable		

Table 6.5 Module Bus Pin Assignments

Function Performed: Input Received Character	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11 A10 A9 A4)	X	ADDR 12
Switch Selectable	A11	ADDR 11
Data Comm = (1110)	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR5 = 0	X	ADDR 8
ADDR6 = 0	X	ADDR 7
	0	ADDR 6
	0	ADDR 5
Data Bus Bit Interpretation:	A4	ADDR 4
	X	ADDR 3
B7	X	ADDR 2
Input Data Bit 7	X	ADDR 1
	X	ADDR 0
	B7	BUS 7
B6	B6	BUS 6
Input Data Bit 6	B5	BUS 5
	B4	BUS 4
B5	B3	BUS 3
Input Data Bit 5	B2	BUS 2
	B1	BUS 1
	B0	BUS 0
B4	1=Logical 1=Bus Low	
Input Data Bit 4	0=Logical 0=Bus High	
	X=Don't Care	
B3		
Input Data Bit 3		
B2		
Input Data Bit 2		
B1		
Input Data Bit 1		
B0		
Input Data Bit 0		

Table 6.6 Module Bus Pin Assignments

Function Performed: Input Status Byte 1 (Interrupt Status)	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11 A10 A9 A4)	X	ADDR 12
Switch Selectable	A11	ADDR 11
Data Comm = (1110)	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR5 = 1	X	ADDR 8
ADDR3 = 0	X	ADDR 7
ADDR6 = 0	0	ADDR 6
	1	ADDR 5
Data Bus Bit Interpretation: An interrupt is generated if any condition causes B0, B1, or B7 to be set to the "1" value. Values of B5 and B6 are valid only is B7 = 1	A4	ADDR 4
	0	ADDR 3
	X	ADDR 2
	X	ADDR 1
	X	ADDR 0
B7	B7	BUS 7
0 = Receiver Register Empty	B6	BUS 6
1 = Receiver Register Full (Cleared by inputting a character or receiver reset)	B5	BUS 5
	B4	BUS 4
B6	B3	BUS 3
0 = No Parity Error	B2	BUS 2
1 = Parity Error (Cleared by inputting status)	B1	BUS 1
	B0	BUS 0
B5	1=Logical 1=Bus Low	
0 = No Overrun Error	0=Logical 0=Bus High	
1 = Overrun Error (Cleared by inputting status or character)	X=Don't Care	

B2

0 = No Fill Character Added to Transmission
1 = Fill Character Transmitted (Cleared by inputting status)

B1

0 = No Timer Interrupt
1 = Timer Interrupt Active (Cleared by resetting timer)

B0

0 = No Transmit Interrupt
1 = Transmit Interrupt Active (Set when CB comes up, cleared by outputting character or dropping CA or CB)

Table 6.7 Module Bus Pin Assignments

Function Performed: Input Status Byte 2 (Modem Status)	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11 A10 A9 A4)	X	ADDR 12
Switch Selectable	A11	ADDR 11
Data Comm = (1110)	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR3 = 1	X	ADDR 8
ADDR5 = 1	X	ADDR 7
ADDR6 = 0	0	ADDR 6
	1	ADDR 5
Data Bus Bit Interpretation:	A4	ADDR 4
	1	ADDR 3
B7	X	ADDR 2
Always 1	X	ADDR 1
Indicates Multipoint PCA in system	X	ADDR 0
	B7	BUS 7
B6	B6	BUS 6
Always 1	B5	BUS 5
Indicates Multipoint PCA in system	B4	BUS 4
B5	B3	BUS 3
0 = CAI On (Downline CA)	B2	BUS 2
1 = CAI Off	B1	BUS 1
	B0	BUS 0
B4		
0 = CE On	1=Logical 1=Bus Low	
1 = CE Off	0=Logical 0=Bus High	
	X=Don't Care	
B3		
0 = SB On		
1 = SB Off		
B2		
0 = CC On		
1 = CC Off		
B1		
0 = CF On		
1 = CF Off		
B0		
0 = CB On		
1 = CB Off		

Table 6.8 Module Bus Pin Assignments

Function Performed: Input Jumper Settings	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (A11 A10 A9 A4)	X	ADDR 12
Switch Selectable	A11	ADDR 11
Data Comm = (1110)	A10	ADDR 10
	A9	ADDR 9
Function Specifier: ADDR5 = 0	X	ADDR 8
ADDR6 = 1	X	ADDR 7
	1	ADDR 6
A3	0	ADDR 5
0 = Select Jumper Character 0 (J00 - J07)	A4	ADDR 4
1 = Select Jumper Character 1 (J10 - J17)	A3	ADDR 3
	X	ADDR 2
Data Bus Bit Interpretation:	X	ADDR 1
	X	ADDR 0
B7-B0 } 0 = Closed Switch	B7	BUS 7
} 1 = Open Switch	B6	BUS 6
	B5	BUS 5
B7	B4	BUS 4
Switch 7	B3	BUS 3
	B2	BUS 2
B6	B1	BUS 1
Switch 6	B0	BUS 0
	1=Logical 1=Bus Low	
B5	0=Logical 0=Bus High	
Switch 5	X=Don't Care	
B4		
Switch 4		
B3		
Switch 3		
B2		
Switch 2		
B1		
Switch 1		
B0		
Switch 0		

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), typical daisy-chain connection (figure 3), components location diagram (figure 4), and the parts list (02640-60107) located in the appendix.

The Synchronous Multipoint Interface PCA block diagram illustrates the major logic sections of the PCA. The key functional block is the LSI Universal Synchronous Receiver/Transmitter (USRT) which serializes and formats data. The module interfaces to the terminal bus with the bus decoder logic and wait logic and is controlled by programs which utilize the interrupt logic and the status and configuration jumpers for input information. The USRT and the control register receive output control information from the program. The RS232C drivers and receivers provide the modem and computer interface for the module, while the daisy-chain drivers and receivers are used for connecting to other terminals with synchronous interfaces. The interface control logic is under program control and provides down line control and special monitor mode function.

3.1 UNIVERSAL SYNCHRONOUS RECEIVER/TRANSMITTER (USRT).

3.1.1 The USRT is a large scale integrated circuit (LSI) which performs synchronous serial data transmission, data formatting, and input and output buffering. The USRT also provides status on both received data and transmitted data. The USRT contains internal registers which hold character size and parity control information, transmit fill character, and receive sychronization character. Data is shifted into and out of the USRT by transmit and receive clocks from the interface.

3.1.2 The USRT (U51) is an American Microsystems Incorporated (AMI) S2350 and provides synchronous serial data formatting and control.

3.1.2.1 The USRT receives eight parallel data inputs ($\overline{BUS7}$ through $\overline{BUS0}$) from the terminal bus through inverters (U41 and U42). The bus decoder logic sends a $\overline{DATA\ OUTPUT}$ signal to the USRT at U51, Pin 38 when an output character is on the terminal bus data lines. The same data input lines are used when the software loads the synchronization character ($\overline{SYNC\ OUTPUT}$) into the USRT at U51, Pins 23 and 24. The synchronization character is used by the USRT as a fill character during serial transmission and as an input synchronizing pattern on receive.

3.1.2.2 The USRT also receives four control inputs (U51, Pin 40, 39, 3, and Pin 4) which determine character size and parity. These four bits correspond to terminal bus data signals $\overline{BUS7}$ through $\overline{BUS4}$. The control bits are loaded into the USRT at U51, Pin 5 by $\overline{CHAR\ CONTROL}$ from the bus decoder logic. Refer to table 6.2 for a definition of the control bits.

3.1.2.3 When a character has been received by the USRT it is available in parallel at the outputs of the USRT (U51, Pins 26 through Pin 33). An Input Data command from the bus decoder logic gates the character to the terminal bus through buffers (U43 and U44).

3.1.2.4 The USRT has two reset signals which initialize the operation of the device. RESET (U51, Pin 14) is used to clear the entire USRT when it is high. This input is driven by the terminal bus PWR ON signal after it is inverted at U35, Pin 4. The other signal is $\overline{RR}$ (Receiver Reset) at U51, Pin 13 and it initializes the receiver portion of the USRT only when it is made low by the bus decoder logic. The receiver reset function clears all receiver status and puts the USRT into the serial input synchronization mode, where the synchronization character is matched with all input to achieve character framing.

3.1.2.5 The USRT provides several status outputs used by the module for controlling data input and output. For data output TBMT (Transmit Buffer Empty) at U51, Pin 9 indicates when the USRT is ready for another parallel data character from the terminal bus. TBMT will be high until a character is loaded into the USRT at U51, Pin 38. A character can be loaded into the buffer register on the USRT while another is being serially transmitted. If a character has not been loaded into the USRT by the time the character being transmitted is finished, then the synchronization character will be substituted and transmitted until a data character is loaded. This is indicated by FCT (Fill Character Transmitted) at U51, Pin 7 which is returned as status. When data has been received, the USRT makes RDA (Received Data Available) at U51, Pin 12 high and a character is ready at the parallel outputs. Also, RPE (Receiver Parity Error) and ROR (Receiver Overrun) at U51, Pin 10 and 11, respectively are valid character status available to the software. If a character is not input before another is received, the ROR status will go high. RDA is made low when a character is input ($\overline{RDE}$) at U51, Pin 35 by the bus decoder logic. Receiver Reset clears RDA, RPE, and ROR while a status input ($\overline{SWE}$) at Pin 34 clears only RPE and ROR.

3.1.2.6 Serial data output from the USRT (TSO) at U51, Pin 6 is controlled by a clock input TCP (Transmit Clock) at U51, Pin 36. $\overline{\text{DATA OUTPUT}}$ is changed on the low to high transition of the clock, which is equal to the transmit frequency or baud rate. Data is shifted out of the USRT least significant bit first and the most significant bit last. (The parity bit could be the MSB.) Serial data input is received by the USRT (RSI) at U51, Pin 25 and controlled by Receive Clock (RCP) at U51, Pin 37. RSI is sampled by the high to low transition of the Receive Clock. Both clocks are inputs to the USRT from the interface (either RS232C or daisy-chain).

3.2 BUS DECODER LOGIC.

3.2.1 The bus decoder logic recognizes and decodes input and output commands directed to the Synchronous Multipoint Interface PCA. Configuration switches set the PCA I/O address and a comparator and additional terminal bus control inputs enable the input and output commands. The various commands are decoded and are used to control the function of the module.

3.2.2 The bus decoder logic consists of an address comparator (U46) and configuration jumpers and a 1-of-8 decoder (U47). All of the input and output commands for the PCA are decoded by interpreting terminal bus address and control lines.

3.2.2.1 The address comparator and address configuration jumpers determine the I/O address of the PCA. When an $\overline{\text{I/O}}$ command is active on the bus (P1, Pin 21 is low) the comparator determines whether the module address is equal or not. If the module address is equal to the address on the bus ($\overline{\text{ADDR11}}$, $\overline{\text{ADDR10}}$, $\overline{\text{ADDR9}}$, and $\overline{\text{ADDR4}}$) and $\overline{\text{REQ}}$ is made low, ADDRESS EQUAL goes high (U47, Pin 6) enabling the decoder and the wait logic.

3.2.2.2 The 1-of-8 decoder receives $\overline{\text{WRITE}}$, $\overline{\text{ADDR6}}$, and $\overline{\text{ADDR5}}$ from the terminal bus to decode input and output commands. $\overline{\text{ADDR3}}$ is also used to decode certain commands. The following is a summary of the commands. Tables 6.0 through 6.8 explain the details of the commands.

SIGNAL	SOURCE
$\overline{\text{INPUT DATA}}$	U47, Pin 7
$\overline{\text{INPUT STATUS}}$	U47, Pin 9
$\overline{\text{INPUT SWITCHES}}$	U47, Pin 10
$\overline{\text{CONTROL OUT}}$	U47, Pin 12
$\overline{\text{CHAR CONTROL}}$	U47, Pin 13
$\overline{\text{LOAD CONTROL REGISTER}}$	U47, Pin 14
$\overline{\text{LOAD CHAR}}$	U47, Pin 15
$\overline{\text{DATA OUTPUT}}$	U36, Pin 8
$\overline{\text{SYNC OUTPUT}}$	U36, Pin 6

The two inputs ($\overline{\text{INPUT SWITCHES}}$ and $\overline{\text{INPUT STATUS}}$) are combined into one enable command (STATUS ENABLE) at U37, Pin 8 which gates the information to the terminal bus. Whenever the USRT status is input, $\overline{\text{SWE}}$ at U51, Pin 34 is pulsed low by U45, Pin 3 to clear character status after it has been input by the software. $\overline{\text{CONTROL OUT}}$ is further decoded into three signals, RECEIVER RESET (U45, Pin 11), TIMER ON (U45, Pin 8), and TIMER OFF (U45, Pin 6).

3.3 WAIT LOGIC. When an I/O command is enabled by ADDRESS EQUAL (U58, Pin 3), the wait logic provides a 600 nanosecond timing cycle which extends the terminal bus cycle so that all timing requirements of the USRT inputs and outputs are satisfied. When the module is not address, two flip-flops (U25, Pins 8 and 6) are both reset. When ADDRESS EQUAL goes high, the two flip-flops will count the next three SYS CLK inputs and stop when both are set. Until both flip-flops are set $\overline{\text{WAIT}}$ (U58, Pin 6) is held low. $\overline{\text{WAIT}}$ is brought high when U37, Pin 3 goes low as a result of both flip-flops being set.

3.4 STATUS AND SOFTWARE CONFIGURATION SWITCHES.

3.4.1 The Synchronous Multipoint Interface PCA has four available status bytes (eight bits) which are input commands enabled by the bus decoder logic. Two of these status bytes correspond to software configuration switches on the PCA (labeled J17 through J10 and J07 through J00) which are given their meaning by the software programs that control the module. One of the bytes gives interrupt and USRT status information. The last status byte gives interface signal status and has two bits which identify the module to the software.

3.4.2 The status and software configuration switches consist of two 8-position rocker switches with pullup resistors and four multiplexers (U12, U13, U22, and U23). Details of the status inputs can be found in tables 6.6 through 6.8.

3.4.2.1 The bus decoder logic provides a STATUS ENABLE signal (U37, Pin 8) when one of the four input commands are received. This gates data from the multiplexers to the terminal bus through buffers (U11 and U21). $\overline{\text{ADDR6}}$, $\overline{\text{ADDR5}}$, and $\overline{\text{ADDR3}}$ determine which of the four inputs are enabled.

DESCRIPTION	$\overline{\text{ADDR6}}$	$\overline{\text{ADDR5}}$	$\overline{\text{ADDR3}}$
Input Interrupt Status	0	1	0
Input Modem Status	0	1	1
Input Switches 0	1	0	0
Input Switches 1	1	0	1

3.4.2.2 The multiplexers (U12, U13, U22, and U23) are dual 4-to-1 multiplexers with common select inputs (Pins 2 and 14). When any of the switches are open, the input to the multiplexer will be high and a "1" will be returned in the switch status bit (closed is a low or "0"). The other status inputs come from the USRT, the interrupt logic, and the interface. Inputs U23, Pin 13 and 3 are always high indicating that the Synchronous Multipoint Interface PCA is present.

3.5 CONTROL REGISTER. The control register (U31) is loaded from the terminal bus by the bus decoder logic signal LOAD CONTROL REGISTER (U47, Pin 14). Six data bits (BUS7, and BUS4 through BUS0) are loaded from the terminal data bus. (Refer to table 6.3 for individual bit assignments). Four of the bits of the control register directly control interface outputs. One bit (U31, Pin 5) controls the monitor mode function and is enabled by a high. The last bit (DOWNLINE INHIBIT) at U31, Pin 2 controls daisy-chain inputs and when high inhibits downline signals under software control (see section 3.7.2.1). One input to the register comes directly from terminal bus signal BUS0 and is inverted by U39, Pin 3 before controlling the interface. This allows the control register to be reset (U31, Pin 1) with CA being low at the interface while the reset of the control signals are high. Monitor mode is disabled and downline signals (DOWNLINE DATA and DOWNLINE REQUEST TO SEND) are enabled when the control register is reset.

3.6 INTERRUPT LOGIC.

3.6.1 The interrupt logic enables the PCA to make the terminal bus ATN line low signaling a need for service by the control software. The interrupts from the Synchronous Multipoint Interface PCA are RECEIVE DATA, TRANSMIT INTERRUPT, and TIMER INTERRUPT. The TRANSMIT INTERRUPT is active only when the USRT can accept another output character and the module has set its REQUEST TO SEND control bit (U31, Pin 15) and has received CLEAR TO SEND (CB) from the interface. The TIMER INTERRUPT is present whenever a timing cycle of 45 milliseconds has been triggered and completed before being reset. The RECEIVE DATA means that data is available at the USRT outputs and status for that character is also available.

3.6.2 The interrupt logic consists of a one-shot timer (U24) a Timer flip-flop (U34, Pin 6), a Last Character flip-flop (U34, Pin 8), and additional logic. The $\overline{ATN}$ signal is pulled low whenever an interrupt condition exists.

3.6.2.1 The USRT signal RDA (Received Data Available) at U51, Pin 12 will cause an interrupt any time a character has been received. RDA is made low and the interrupt condition cleared whenever the software inputs the character ($\overline{RDE}$) at U51, Pin 35.

3.6.2.2 The one-shot timer is provided by the PCA so that software for the module can be totally interrupt driven. The one-shot (U24) provides a 45 millisecond timing interval when triggered by the $\overline{CONTROL\ OUT}$ command TIMER ON (U45, Pin 8). When the one-shot starts its timing cycle the Timer flip-flop is set on the next SYS CLK. When the one-shot finishes its timing cycle U24, Pin 6 will go high and a TIMER INTERRUPT will be present (U33, Pin 6). If the software does not need a complete 45 millisecond period it can clear both the one-shot and Timer Flip-flop by outputting a TIMER OFF (U45, Pin 6). PWR ON also clears the timer function.

3.6.2.3 The USRT can also interrupt when it is ready to load another character for transmission. When REQUEST TO SEND (U31, Pin 15 of the control register) is low and $\overline{CLEAR\ TO\ SEND}$ (U29, Pin 12) is low TBMT will cause an interrupt. The interrupt is detected by U32, Pin 9, Pin 10 (Last Character flip-flop off) and Pin 11. These conditions cause an INTERRUPT signal at U37, Pin 6 and return a status bit at U42, Pin 6. The TRANSMIT INTERRUPT can be modified by the Last Character flip-flop to indicate that the last character has been completely shifted out of the USRT. By setting the Last Character flip-flop, the normal TBMT interrupt is disabled and an interrupt will occur only when FCT at U51, Pin 7 goes high. This means that no new character was loaded and the last data character is finished. The Last Character flip-flop is set by $\overline{CONTROL\ OUT}$ with $\overline{ADDR7}$ on (low) and reset with $\overline{ADDR3}$ on (low).

3.7 INTERFACE CONTROL.

3.7.1 The interface control logic enables the PCA to control daisy-chain sharing of a serial data transmission line and to perform a line monitoring function. DOWNLINE INHIBIT (U31, Pin 2) from the control register prevents down line terminals from interfering if a terminal wants to transmit data on a shared line. The MONITOR MODE ENABLE (U31, Pin 5) bit from the control register enables a multiplexer to select either received data from the interface (from a computer or modem) or transmit data from terminals down line. This enables the monitoring terminal to receive data and clock from the interface for the direction of data flow. A Transmit Buffer flip-flop is present to allow time for TRANSMIT CLOCK and TRANSMIT DATA to propagate up and down a daisy-chain connection.

3.7.2 The interface control logic consists of a line monitor multiplexer (U28), a Transmit Buffer flip-flop (U27), and down line inhibit gates. The downline inhibit and monitor mode functions are under software control by loading the control register.

3.7.2.1 The line monitor multiplexer is used to select the source of the USRT input data and clock (RSI and RCP). When monitor mode is disabled (U28, Pin 2 is low) the multiplexer will gate data and clock to RCP and RSI of the USRT. when monitor mode is enabled (U28, Pin 2 is high) DOWNLINE REQUEST TO SEND (CAI) controls the multiplexer (U28, Pin 14) and selects either RECEIVE DATA and RECEIVE CLOCK or DOWNLINE DATA (BAI) at U39, Pin 10 and TRANSMIT CLOCK (DD or DBI). when DOWNLINE REQUEST TO SEND is low the USRT will receive the data coming up the daisy-chain from other terminals. When DOWNLINE REQUEST TO SEND is high the USRT will receive data and clock from the modem or computer interface. This allows passive monitoring of both directions in a half duplex protocol.

3.7.2.2 When the Synchronous Multipoint Interface PCA is in a daisy-chain configuration and sharing a line with other terminals, it must disable all terminals down line when it wants to transmit data. This is done by

making U31, Pin 2 high which keeps CLEAR TO SEND from going down the daisy-chain at U38, Pin 8 and DOWNLINE DATA (BAI) at U36, Pin 11 and DOWNLINE REQUEST TO SEND (CAI) at U38, Pin 3 from going up the daisy-chain. This feature is used by the software to eliminate interference between daisy-chained terminals under certain contention conditions.

3.7.2.3 The Transmit Buffer flip-flop receives serial data from the USRT and the downline terminals (BAI). The two data streams are merged by U37, Pin 11. Data from downstream is controlled by DOWNLINE INHIBIT and data from the USRT is controlled by CLEAR TO SEND and REQUEST TO SEND. Only one of the two inputs will be active. The flip-flop clocks data in on the rising edge of the Transmit Clock (U29, Pin 4) and sends its output to RS232C output BA (U18, Pin 8). This allows data down stream to have one full bit time to change and settle before it is sent to a modem or computer. The daisy-chain data going up the daisy-chain does not use the Transmit Buffer flip-flop so that only the first terminal in the chain uses this function.

3.8 SYNC CLOCK GENERATOR.

3.8.1 The sync clock generator provides compatible synchronous clocks to the RS232C interface by dividing the terminal bus SYS CLK with a divider chain. A set of switches allow one of four data rates to be selected. The PCA can receive both transmit and receive clocks from a modem or computer (hardwired) or supply one or both of the required clocks.

3.8.2 The sync clock generator consists of a divider chain (U16 and U26) and rate selection jumpers. Normally, the PCA will transmit and receive clock inputs from a modem. When a modem requires a transmit clock (RS232C signal DA) or a computer requires both transmit and receive clock, the PCA can supply both. The clock is also used in self-test loop-back of interface signals.

3.8.2.1 The synchronous clock rates are derived by dividing the terminal SYS CLK (4.915 MHz) by powers of two. A divide-by-16 counter (U26) and a dual divide-by-16 counter (U16) provide this function. The five outputs of U16 give the rates of 1200 (not switch selectable), 2400, 4800, 9600, and 19200, which are times one clocks. Only one of the clock rates should be selected at a time (switch closed) or U16 might be damaged as a result of the two outputs being tied together.

3.8.2.2 The first divide-by-16 counter has a test point (CNTLD) which can be used by an automatic tester to decrease the number of patterns needed to test U16. By pulling CNTLD low, the counter presets to seven and then can be counted up to eight.

3.9 RS232C DRIVERS.

3.9.1 The Synchronous Multipoint Interface PCA provides an RS232C compatible interface on the P2 connector by using integrated circuit buffers U18 and U110.

3.9.2 Each RS232C signal has a 330 picofarad slew-rate capacitor on the output. Four of the signals come directly from the control register (CA, CD, CH, SCA) and are under software control. Transmit Data (BA) comes from the USRT or the daisy-chain logic of terminals down line. The Transmit Clock RS232C signal, DA (U18, Pin 3) is available at the interface for either modem or hardwired connections. An additional clock (RCLK) is switch selectable and provides a receive clock for the terminal (DD) at U210, Pin 1 in direct connections to computers. The RCLK signal is enabled when CF (U210, Pin 3) is high with Q13 acting as a discrete component implementation of an inverter.

3.10 RS232C RECEIVERS.

The RS232C compatible interface has eight inputs which are buffered by integrated circuit receivers (U19 and U210). Four of the input signals (CC, CF, CE, and SCF) go directly to the status multiplexers and are used by the software for modem control. The other four RS232C inputs (BB, CB, DB, and DD) are logically ORed with the daisy-chain receivers. Normally, the first terminal in a daisy-chain connection of 264X terminals with Synchronous PCA's will receive RS232C signals while the daisy-chain receivers are not connected. The PCA then buffers all the signals and sends them down the daisy-chain and the other RS232C interfaces will be unconnected and the daisy-chain receivers will be active. Refer to figure 3 for typical connection of daisy-chain signals.

3.11 DAISY-CHAIN DRIVERS.

The daisy-chain connection of terminals using the Synchronous Multipoint Interface PCA requires special drivers. These special drivers buffer signals which are received and send them up or down the daisy-chain connection. The six drivers are four signals (BBO, CBO, DBO, and DDO) going away from the modem or computer and two signals (BAO and

CAO) going towards the first terminal in the chain. The drivers consist of peripheral driver integrated circuits (U48, U59, and U410) and discrete components. All drivers are the same with Q1, Q3, Q5, Q7, Q9, and Q11 being turned on when open-collector peripheral driver is off. Q2, Q4, Q6, Q8, Q10, and Q12 provide short circuit protection from momentary shorts. The special drivers provide a high current drive of +12 volts for the opto-isolated receivers.

3.12 DAISY-CHAIN RECEIVERS.

The daisy-chain receivers are optical isolator receivers which provide ground isolation between the driving terminal and the receiving terminal. The six inputs are divided into two groups of signals. The group of inputs from a driving terminal up the daisy-chain are BBI, CBI, DBI, and DDI and they all share the same ground return of RET-U (P2, Pin 10). The other group of two is BAI and CAI which share ground return RET-D (P2, Pin 8). The opto-isolator (U111, U112, U211, U310, U311, and U312) is on when current flows in the input diode (output is low) and off when no current flows. The 470-ohm resistors limit the input current from the drivers to less than 25 milliamperes. The opto-isolator requires 16 milliamperes of forward current to make the output go on. The four inputs (BBI, CBI, DBI, and DDI) are logically ORed with the RS232C receivers (U29).

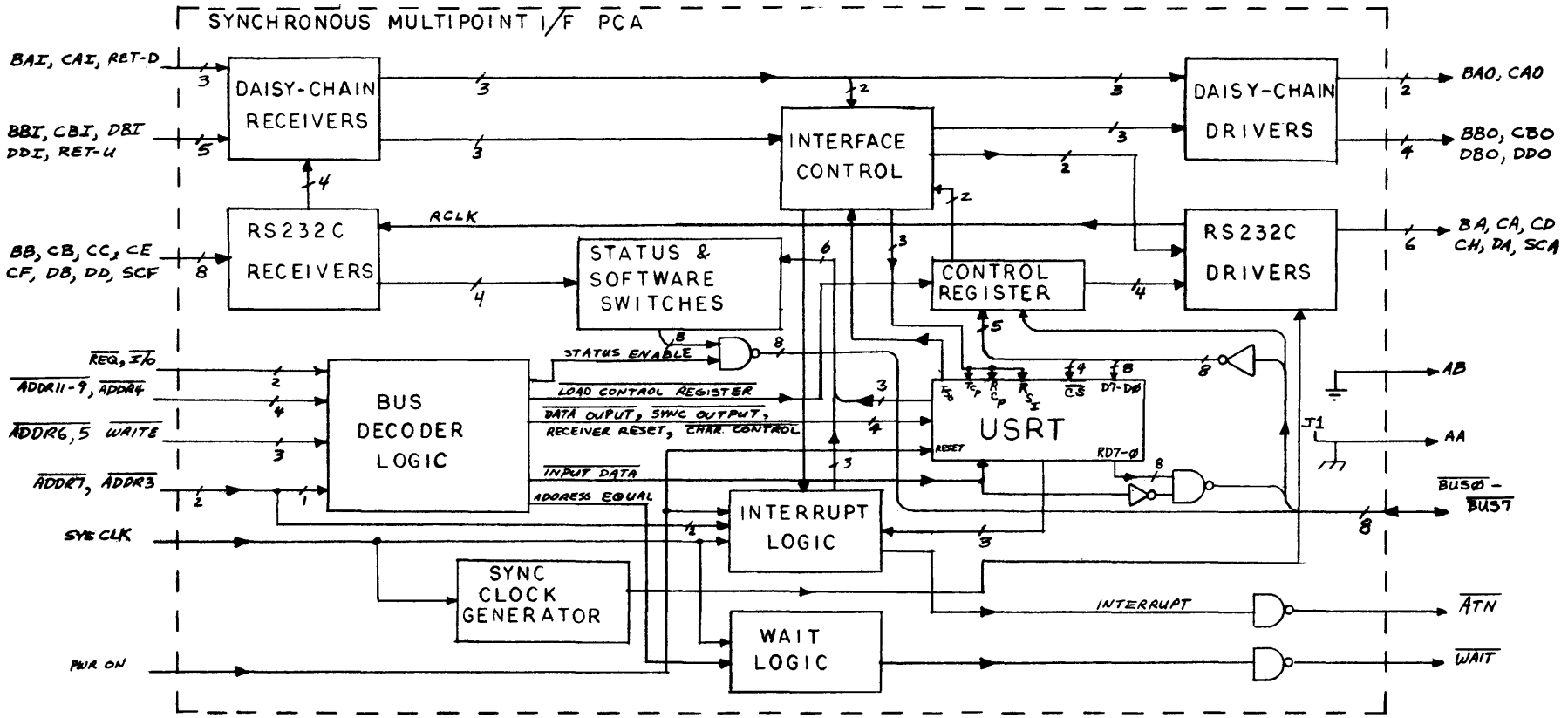

Figure 1
Synchronous Multipoint Interface Block Diagram
AUG-01-76 13255-91107

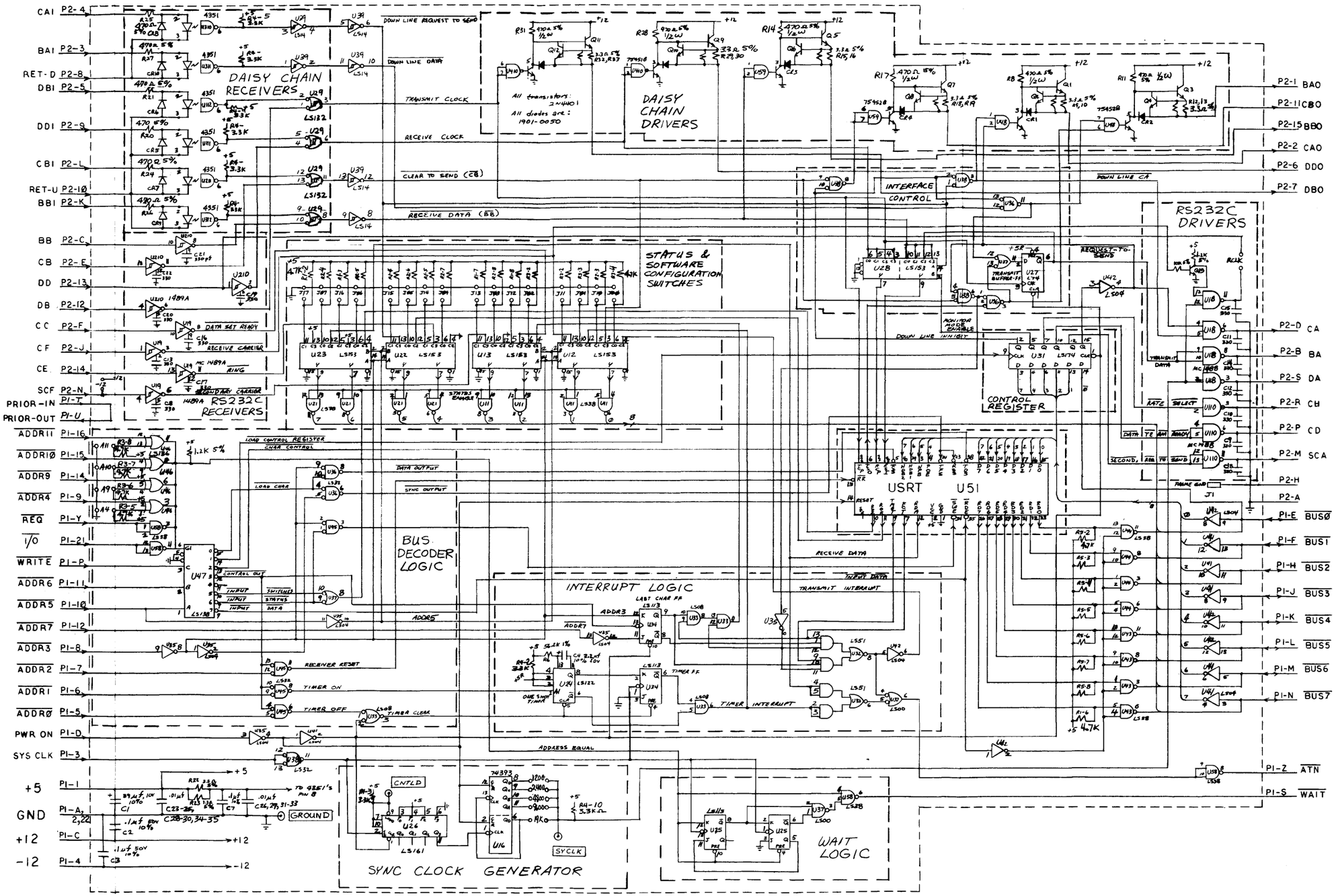

Figure 2
Synchronous Multipoint Interface PCA
Schematic Diagram
AUG-01-76 13255-91107

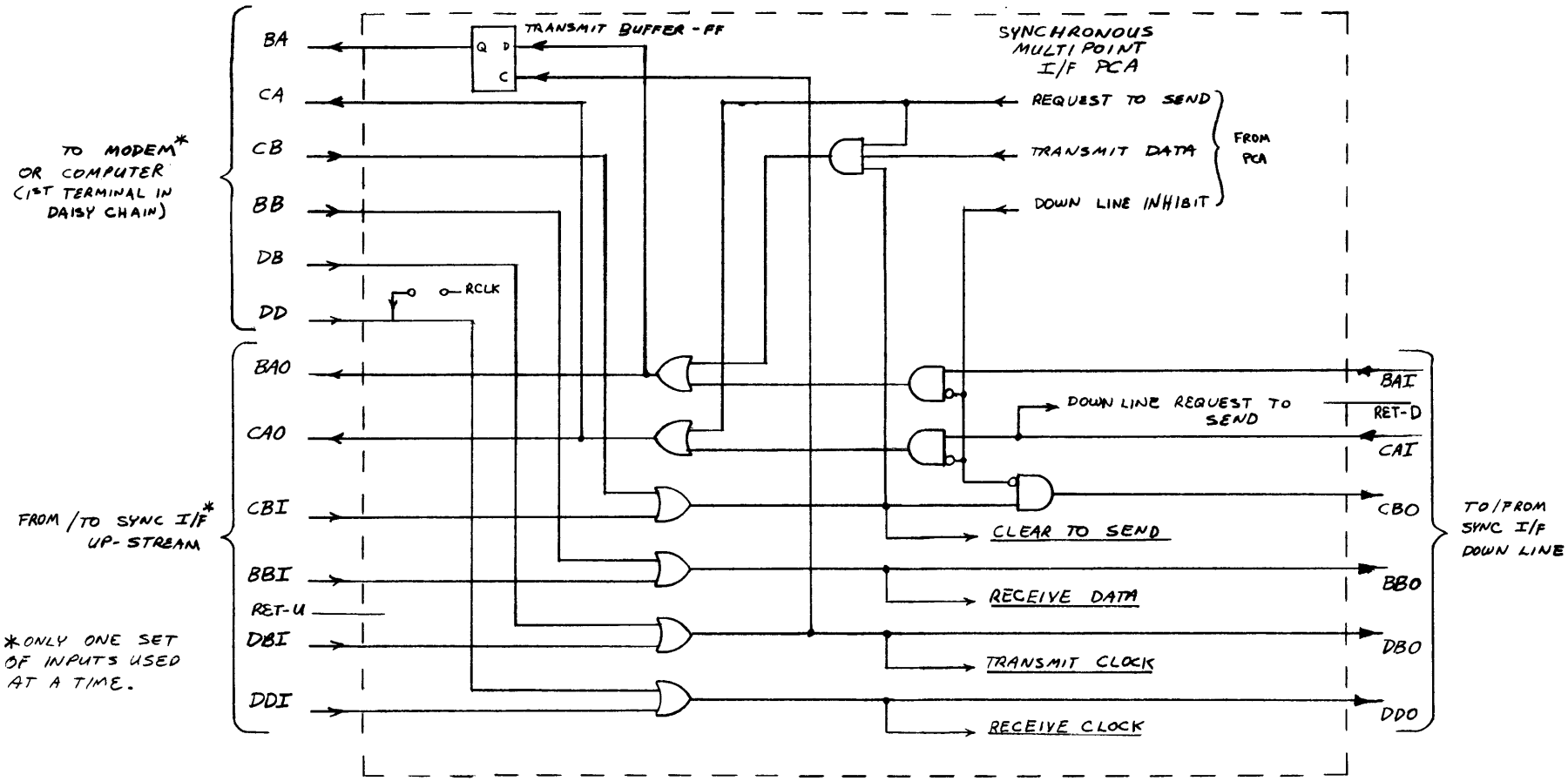

Figure 3
Typical Daisy-Chain Connection Diagram
AUG-01-76 13255-91107

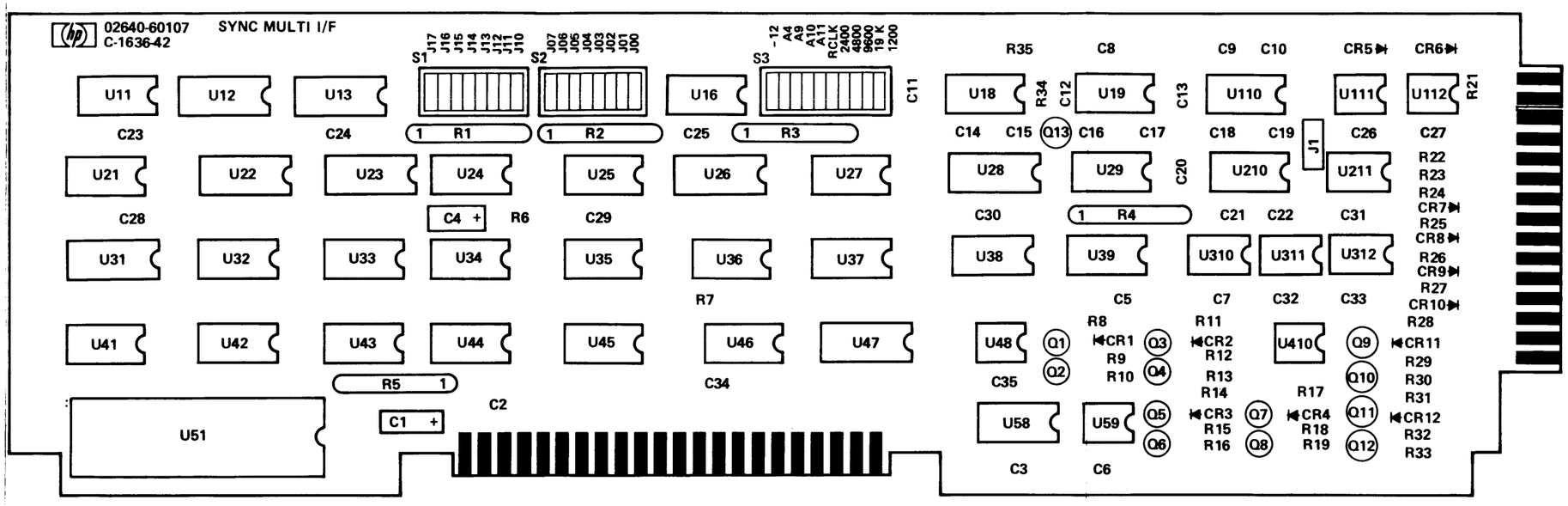

Figure 4
Synchronous Multipoint Interface PCA
Component Location Diagram
AUG-01-76 13255-91107

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60107	1	SYNC MULTIPOINT INTERFACE ASSEMBLY DATE CODE: B-1636-42 REVISION DATE: 10-23-76	28480	02640-60107
C1	0180-0393	1	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0150-0121	5	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C3	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C4	0180-0197	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C5	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C6	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C7	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C8	0160-3572	15	CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C9	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C10	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C11	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C12	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C13	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C14	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C15	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C16	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C17	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C18	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C19	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C20	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C21	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C22	0160-3572		CAPACITOR-FXD 330PF +-10% 500WVDC CER	28480	0160-3572
C23	0160-2055	13	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C24	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C25	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C26	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C27	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C28	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C29	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C30	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C31	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C32	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C33	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C34	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C35	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
CR1	1901-0050	12	DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR2	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR3	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR4	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR5	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR6	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR7	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR8	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR9	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR10	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR11	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
CR12	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
E1	0360-0124	3	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
J1	1251-1126	1	CONNECTOR-SGL CONT SKT .08-IN-BSC-SZ RND	74970	105-0754-001
Q1	1854-0467	13	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q2	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q3	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q4	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q5	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q6	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q7	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q8	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q9	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q10	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q11	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q12	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
Q13	1854-0467		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	04713	2N4401
R1	1810-0125	4	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R2	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R3	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R4	1810-0278	1	NETWORK-RES		
R5	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R36	0683-1025	4	RESISTOR 1000 5% .25W		
R37	0683-1025		RESISTOR 1000 5% .25W		
R38	0683-1025		RESISTOR 1000 5% .25W		
R39	0683-1025		RESISTOR 1000 5% .25W		

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			SYNC MULTIPOINT INTERFACE ASSEMBLY CONT'D.		
R6	0757-0459	1	RESISTOR 56.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5622-F
R7	0683-1225	2	RESISTOR 1.2K 5% .25W FC TC=-400/+700	01121	CB1225
R8	0686-4715	6	RESISTOR 470 5% .5W CC TC=0+529	01121	EB4715
R9	0683-0335	14	RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R10	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R11	0686-4715		RESISTOR 470 5% .5W CC TC=0+529	01121	EB4715
R12	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R13	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R14	0686-4715		RESISTOR 470 5% .5W CC TC=0+529	01121	EB4715
R15	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R16	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R17	0686-4715		RESISTOR 470 5% .5W CC TC=0+529	01121	EB4715
R18	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R19	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R20	0683-4715	6	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R21	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R22	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R23	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R24	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R25	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R26	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R27	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R28	0686-4715		RESISTOR 470 5% .5W CC TC=0+529	01121	EB4715
R29	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R30	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R31	0686-4715		RESISTOR 470 5% .5W CC TC=0+529	01121	EB4715
R32	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R33	0683-0335		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
R34	0683-1225		RESISTOR 1.2K 5% .25W FC TC=-400/+700	01121	CB1225
R35	0683-1035	1	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
S1	3101-2094	2	SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	28480	3101-2094
	3131-0392	2	COV-RKR 0.922 IN LG; 0.422 IN W; 0.217	28480	3131-0392
S2	3101-2094		SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	28480	3101-2094
	3131-0392		COV-RKR 0.922 IN LG; 0.422 IN W; 0.217	28480	3131-0392
S3	3101-2102	1	SWITCH-TGL DIP ROCKER ASSEMBLY 10-1A NS	28480	3101-2102
	3131-0397	1	SWITCH COVER, 10-POSITION	28480	3131-0397
U11	1820-1209	5	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U12	1820-1244	5	IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
U13	1820-1244		IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
U16	1820-1464	1	IC-DIGITAL SN74393N TTL DUAL 8IN	01295	SN74393N
U18	1820-0509	2	IC-DIGITAL MC1488L DTL QUAD LINE	04713	MC1488L
U19	1820-0990	2	IC-DIGITAL MC1489AL DTL QUAD NAND	04713	MC1489AL
U21	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U22	1820-1244		IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
U23	1820-1244		IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
U24	1820-1422	1	IC-DIGITAL SN74LS122N TTL LS	01295	SN74LS122N
U25	1820-1213	2	IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U26	1820-1818	1	IC, DIGITAL 74LS161	28480	1820-1818
U27	1820-1112	1	IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U28	1820-1244		IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
U29	1820-1425	1	IC-DIGITAL SN74LS132N	01295	SN74LS132N
U31	1820-1196	1	IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
U32	1820-1210	1	IC-DIGITAL SN74LS51N TTL LS DUAL 2	01295	SN74LS51N
U33	1820-1201	1	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U34	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U35	1820-1199	3	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U36	1820-1208	3	IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U37	1820-1197	1	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U38	1820-1208		IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U39	1820-1416	1	IC-DIGITAL SN74LS14N TTL LS HEX 1 INV	01295	SN74LS14N
U41	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U42	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U43	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U44	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U45	1820-1208		IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U46	1820-1215	1	IC-DIGITAL SN74LS136N TTL LS QUAD 2	01295	SN74LS136N
U47	1820-1216	1	IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
U48	1820-0799	2	IC-DIGITAL SN75452BP TTL DUAL 2 NAND	01295	SN75452BP
U51	1820-1754	1	IC-DIGITAL S2350 MOS	31471	S2350
U58	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U59	1820-0799		IC-DIGITAL SN75452BP TTL DUAL 2 NAND	01295	SN75452BP
U110	1820-0509		IC-DIGITAL MC1488L DTL QUAD LINE	04713	MC1488L
U111	1990-0444	6	OPTO-ISOLATOR LED-PDIO/XSTR IF=25MA-MAX	28480	1990-0444
U112	1990-0444		OPTO-ISOLATOR LED-PDIO/XSTR IF=25MA-MAX	28480	1990-0444
U210	1820-0990		IC-DIGITAL MC1489AL DTL QUAD NAND	04713	MC1489AL
U211	1990-0444		OPTO-ISOLATOR LED-PDIO/XSTR IF=25MA-MAX	28480	1990-0444

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			SYNC MULTIPOINT INTERFACE ASSEMBLY CONT'D.		
U310	1990-0444		OPTO-ISOLATOR LED-PDIO/XSTR IF=25MA-MAX	28480	1990-0444
U311	1990-0444		OPTO-ISOLATOR LED-PDIO/XSTR IF=25MA-MAX	28480	1990-0444
U312	1990-0444		OPTO-ISOLATOR LED-PDIO/XSTR IF=25MA-MAX	28480	1990-0444
U410	1820-0535	1	IC-DIGITAL SN754518P TTL DUAL 2 AND	01295	SN754518P
	1200-0552	1	SOCKET-IC 40-CONT DIP-SLDR	28480	1200-0552